

METHODS, CIRCUITS, AND SYSTEMS FOR UTILIZING IDLE TIME IN  
DYNAMIC FREQUENCY SCALING CACHE MEMORIES

ABSTRACT

5           Dynamic Frequency Scaling (DFS) cache memories that can be accessed  
during an idle time in a single low frequency DFS clock cycle are disclosed. The  
access can begin during the idle time in the single low frequency DFS clock cycle and  
may continue during a subsequent low frequency DFS clock cycle. The idle time can  
be a time interval in the single low frequency DFS clock cycle between completion of  
10 a single high frequency DFS clock cycle and completion of the single low frequency  
DFS clock cycle. Related circuits and systems are also disclosed.